# Investigation of Thermal Performance of Various Power-Device Packages

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**Abstract**

Continuing trends of miniaturization, rising switching frequencies and increasing packaging densities require increased current handling capability of packaged devices in applications related to power conversion. Traditionally, these ever-increasing demands are met by improvements in silicon efficiency. Nevertheless, with silicon efficiency pushed to the limit, major semiconductor power-device manufacturers are now looking for innovative packaging options for power devices to achieve the next level of breakthroughs in electrical and thermal performance. This paper presents a comprehensive study of thermal behaviors of various power-device packages. CFD-based FLOTHERM has been applied to calculate the junction-to-ambient thermal resistance with the industry standard-specified board attachment. Fundamental cooling mechanisms associated with different packaging technologies, including wire-bond, strap bonding, flip chip and ball grid array (BGA), and wafer-level packaging are investigated. The impact of internal package design on the thermal performance of various packages is discussed in detail. A thermal analysis of multichip module for leadless and BGA technologies is also presented.

**Introduction**

Applications demanding high-power conversion such as voltage regulator module for microprocessors, automotive electronics and telecommunications, have introduced a trend for achieving higher power densities at lower cost [1,2]. Over the past decades, this trend has been successfully met by increasing silicon efficiency; however, future requirements dictate further improvement in overall system efficiency, which can only be achieved through innovations in packaging [3-5]. Accordingly, in recent years, semiconductor industry has taken aggressive steps towards achieving small form factor power packages with significant improvements in electrical and thermal performance. From traditional plastic injection-molded and wire-bonded package, power packaging has come a long way where state of the art IC packaging techniques such as ball-grid-array, chip-scale packaging and leadless, and wafer-level packaging are being used [6-9].

Leaded packages such as TO-220s and axial leaded devices had been the packaging configurations of power devices for the longest time. However, as miniaturization and functional integration became the dominant drivers for electronics components and modules, new technologies emerged[2]. The DPAK package was introduced first in mid-1980, which caused a major paradigm shift in the package design arena. At the same time, an alternative package with SOT-223 came along, which offered smaller outline than DPAK yet used the footprint and pin-outs. Then came D2PAK in the early 1990s, which offered usage of bigger die size in a package, thus increasing current handling capability significantly and reducing thermal resistance of the package to some extent. The SO-8 packages were introduced in the mid-1990, which allowed significant size reduction compared to DPAK packages and resulted in fewer packages required for assembly while reducing board space. This improvement was made possible since the die size reduction and more cells per inch of silicon enabled designers to achieve the same type of RDS(on) performance in SO-8, which was previously only available in TO-220 and DPAK configurations [8].

However, continued miniaturization drive demanded even smaller and more efficient package than SO-8 packages to meet future thermal and electrical

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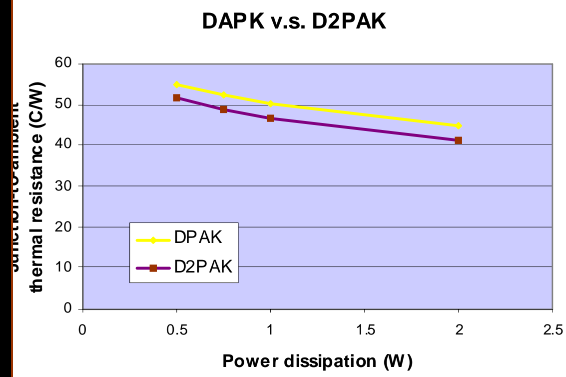
(TQFPs) b using a 3-D finite element scheme. A methodology for low profile 48-lead TQFPs was outlined. Ganesa-Pillai and Chen [14] presented a finite-element thermal analysis of a boost converter module, which integrated all the semiconductor devices and the snubber circuits of a boost converter on a ceramic substrate. The effects of different substrates and use of multiple current sharing components were examined. Katsis and Van Wyk [15] compared the thermal impedance of modules with varying void area at a constant power dissipation level in order to develop a relationship between thermal impedance and void area. The effect of aging on thermal transient behavior was correlated to finite element thermal simulations. Chiriac and Lee [16] performed a detailed thermal analysis for the wirebonded GaAs devices by using numerical simulations. The main focus was on the impact of die attach thermal conductivity, substrate's top metal layer thickness, and via wall thickness on the overall thermal performance of GaAs IC device . Arik Garg, and Bar-Cohen [17] explored the thermal challenges in advanced system-on-package (SOP) electronic structures, as well as candidate thermal solutions for these highly demanding cooling needs. Detailed three-dimensional (3-D) finite-element simulations were used to study the temperature distributions in a typical SOP package, and to provide guidance for the development and implementation of "compact thermal models". Direct liquid cooling by immersion of the components in inert, nontoxic, high dielectric strength perfluorocarbon liquids was seen effective over a range of anticipated SOP power dissipations. Chiriac and Lee [18] performed a detailed numerical study to examine the thermal characteristics of a chip set at the system level. The chip set included the Power Amplifier (PA) module, power management and base-band packages, front-end receiver package and memory. Detailed solid modeling was applied to the PA module with the GaAs (Gallium Arsenide) device bonded to a multi-layer ceramic substrate. Frank [19] discussed two methods of defining the thermal junction-ambient resistance and the commonly used wave solder assembly technology. The test setup and the results of tests done with various packages and transistors were also described. Kandasamy and Subramanyam [20] numerically evaluated the performance of the package different die sizes and apoxy molding compounds at different power levels. The use of heat slug was investigated to identify its effect on heat dissipation for ICi dnt dr4(o)4.6(n f TD4()-6(he.)6.4(o)4.)1.8(n4.6(n fo)s4(p)4.6(45tam)10fn4.6(n f4(o)4.)1.8(n4.6(n fo(

defined as the junction-to-ambient thermal resistance in steady-state, i.e., $R_{j-a}$.

Unless otherwise stated, the package is mounted on 1 in$^2$ of 2 oz copper on FR4 in our following investigations according to the industry standards. The ambient temperature (temperature in chassis) is assumed to be 50 C under the natural convection condition. The effects of the ambient temperature and the air speed (forced convection) on the thermal resistance are also briefly addressed. The FLOTHERM simulation tool has been used for the analysis.

**Modeling**

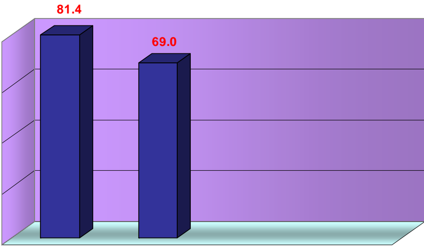



g. 3 Thermal resistance as function of power dissipation for DPAK and D$^2$PAK packages

able 2 Thermal Resistance of DPAK and D$^2$PAK Packages

| | *DPAK* | *D$^2$PAK* |
|---|---|---|
| ***are FR4*** | **186.6** | **104.5** |

leadless, in which the heat dissipation is maximized in one path, the improvement by additional heat path would be insignificant.



the conduction layer (copper) used in BGA as shown in Fig. 10 has negligible effect on thermal resistance. “No conduction layer” in Fig. 11 means that the conduction layer has very low thermal conductivity (~ 0.9 W/Km) which, of course, is not realistic. The results imply that the heat dissipation is dominant through the path of solder balls under the chip. Fig. 11 also shows the effect of underfill on thermal resistance. The improvement is about 12% reduction over the same package without underfill.

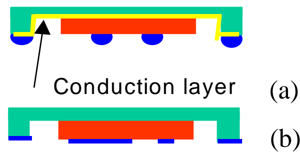
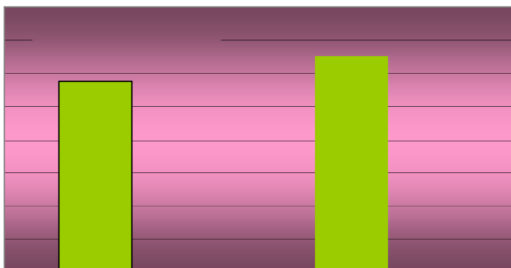



Fig. 10 a): ball grid array (BGA) MOSFET package; b): large contact interconnect MOSFET package

A ball grid array approach, even with multiple balls per connection has a limited contact area with a printed circuit board and hence the thermal performance junction to board and conduction efficiency cannot be maximized. Therefore an underfill material is required in the above applications. An alternate interconnection methodology that addresses this issue has been developed using a large area solder-contact technique. Fig. 12 presents the results of thermal resistance for large contact interconnect compared to the BGA package discussed before. We notice a 10% reduction in thermal resistance over the BGA package.



## Conclusions

Thermal models have been developed for various power-device packages. The CFD-based FLOTHERM simulation tool has been applied to predict the junction-to-air thermal resistance of different packages. It has been found that the difference in thermal resistance between DPAK and D2PAK under the same power dissipation is not significant (less than 5 C/W), in spite of the large differences in die size and package dimensions. This is primary because the package is mounted onto 2oz copper on FR4, which makes the board highly thermal conductive. Due to the large contact area between the copper pad and board, DPAK package displays the least thermal resistance (~50 C/W) and thus sets a baseline to evaluate other types of packages.

SO-8 power packages present a wide range of thermal resistance (50-80 C/W) when different interconnect technology and package format are applied. Strap bonding can improve thermal performance about 15% over the traditional SO-8 power MOSFET. The leadless or micro leadframe package further reduces the thermal resistance to the level comparable to the DPAK, with smaller package dimensions.

Flip-chip-on-board packages or ball grid array (BGA) packages have relatively good thermal performance (50-70 C/W) due to the direct solder interconnect to the board. When underfill is applied, the size and number of solder balls do not matter. However, the thermal performance has strong dependence on the number of solder balls if underfill is not used. The large area contact technology developed maximizes the thermal performance of the flip chip packages to the level of traditional DPAK.

For multichip modules, leadless module achieves better thermal performance (16.9% reduction of thermal resistance) than a similar module using BGA version.

A superior advantage of flip chip packages over wire-bonded packages is the realization of double-sided cooling mechanism. When a heat sink is attached, the thermal behaviors may be completely different from the behaviors shown above. Care must be taken to use the above results in an actual system application either from the predicted thermal resistance or the data from the data sheets, because thermal resistance depends not only on the package design and interconnect, but also on the ambient conditions, heat sink attachment and the board selection.

## References


1. Stephen H. Gunther, Frank Binns, Douglas M. Carmean, and Jonathan C. Hall, Managing the impact of increasing microprocessor power consumption, Intel Technology Journal, Q1, 2001
2. A. Gentchev, DesigninTT11 1 Tfuas11 1 Tfuas11 1 Tfuas11 1 Tfuas11 1 Tfuan(nt)4.9(n)-e Tw9(, Desi)4.3(g)4.9(n)-1unsumond

16. Chiriac, V. A. and Lee, T-Y T., “Impact of die attach material and substrate design on RF GaAs power amplifier devices thermal performance,” ASME Journal of Electronic Packaging, v. 125, pp. 589-596, 2003
17. Arik, M., Garg, J. and Bar-Cohen, A., “Thermal modeling and performance of high heat flux SOP packages,” *IEEE Transactions on Advanced Packaging,* v. 27, pp. 398-412, 2004
18. Chiriac, V. and Lee, T-Y T., “Thermal evaluation of power amplifier modules and RF packages in a handheld communicator system,” ITherm 2004 -